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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,423	08/02/2001	Randhir P.S. Thakur	3978.1US (95-0064.1)	8029

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,423	THAKUR ET AL.	
	Examin r	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/7/3 has been entered.

Response to Amendment

Amendment filed 8/7/3 with said Request for Continued Examination forms the basis of this official action.

In said Amendment Applicant amended claims 1-9, 11 and 12, while claims 10 and 13 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 8/7/3 have been fully considered but they are not persuasive, because, although the amended claim language now explicitly introduces the sidewall of the corrugated capacitor and, consequently, the reference to Ando does no longer make the use of BPSG obvious, BPSG is known as capacitor sidewall material, as evidenced by Ando (6,097,053). Finally, the BPSG and Ge-BPSG layers alternate and abut each other (see Hsia et al, in particular: layers 62 (non-doped) and 64 as depicted in Figure 7), and consequently the traverse on page 9 is moot.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

at least one layer of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

said nonconductive oxide layer with second etching rate having a portion contacting at least a portion of said at least one layer of nonconductive oxide with first etching rate (see abutting layers 62 and 64 in Figure 7 in Hsia);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall in capacitors in the semiconductor device art as evidenced by the description of the prior art by Ando (cf. col. 2, l. 1-14 and Figure 4; in particular BPSG side wall 24, cf. col. 2, l. 4), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at least one layer 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned at least one layer 64.

3. ***Claim 2*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

a plurality of layers of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

at least a portion of at least one layer of said plurality of nonconductive oxide layers with second etching rate contacting at least a portion of at least one layer of said plurality of nonconductive oxide with first etching rate (cf. Figs. 6-8);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall in capacitors in the semiconductor

device art as evidenced by Ando, while BPSG is known for ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures, while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive 64.

4. ***Claim 3*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1);

each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for capacitor side walls in the semiconductor device art as evidenced by the description of the prior art by Ando (cf. Fig. 4, col. 2, l. 1-14) while PBSG is well known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures, while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

5. ***Claim 4*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to

Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

at least one layer of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall material in capacitors in the semiconductor device art as evidenced by Ando, while being known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures, and, furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at

nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

6. ***Claim 5*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-

phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) as the material for capacitor side walls in the semiconductor device art is well known as evident from the description of the prior art in Ando (cf. Fig. 4, col. 2, l. 1-14), while BPSG is widely known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

7. ***Claim 6*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1), each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8);

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) as capacitor side wall material is standard in the semiconductor device art as evidenced by the description of the prior art in Ando, while PSGB is widely known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

8. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising:

at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by at least one layer of nonconductive oxide 62 (cf. column 5, lines 33-35) and at least one layer of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer of nonconductive oxide 62;

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the side wall material in capacitors in the semiconductor device art as evidenced by the description of the prior art by Ando (cf. Fig. 4, col. 2, l. 1-14) while BPSG is widely known for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

9. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a

sidewall surface (cf. Figure 5-8), comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers of nonconductive oxide 62;

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the capacitor side walls in the semiconductor device art as evidenced by the description of the prior art in Ando (cf. Figure 4, col. 2, l. 1-14), while BPSG is widely known to be advantageous for its ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

10. ***Claims 9*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Ando (6,097,053) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, said capacitor cell having a sidewall surface (cf. Figure 5-8), comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), each layer of 64 having at least a portion thereof contacting at least a portion thereof contacting of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62;

at least one layer 26 (cf. Figure 5 and col. 2, l. 2) of dielectric material (polysilicon is a dielectric material) covering at least the sidewall surface of the said capacitor cell; and

at least one electrode layer 28 (cf. col. 2, l. 1-11) deposited over at least a portion of the at least one layer of dielectric material.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the capacitor side wall material in the semiconductor device art as evidenced by the description of the prior art in Ando, while BPSG is widely known to be advantageous because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures. Furthermore, it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

11. ***Claim 11*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Ando, and Haller et al as applied to claim 9 above, and further in view of Kawakubo (5,889,696). As detailed above, claim 9 (on which claim 11 depends) is unpatentable over Hsia et al in view of Ando and Haller et al, neither of whom, however, specifically

teach the semiconductor memory device of claim 9 with the further limitation as defined by claim 11.

However, particularly the use of BST as a high dielectric in capacitors in semiconductor memory devices has long been taught as a means to increase the charge storage capacity of capacitors, as witnessed, for example, by Kawakubo et al, who teach a semiconductor memory device (cf. Abstract, first sentence) with capacitor (cf. Abstract, first sentence) *for the very purpose of achieving very high charge storage* ability through the very high dielectric constant of BST (cf. column 9, lines 58-63). *Therefore, it would have been obvious* to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to include the further limitation of claim 11.

12. ***Claim 12*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Ando, and Haller et al as applied to claim 9 above, and further in view of De Boer et al (5,930,106 and DERWENT copy, under "Novelty"). As detailed above, claim 9 (on which claim 12 depends) is unpatentable over Hsia et al in view of Ando and Haller et al, who, however, do not specifically teach the conductive layer to comprise Si-Ge.

However, Si-Ge has long been taught as semiconductor memory device capacitor electrode material for the purpose of high reliability, as evidenced by De Boer et al, who teach a Si-Ge capacitor plate for the purpose of achieving high reliability (cf. particularly the DERWENT SUMMARY of De Boer et al) in a semiconductor memory device capacitor (cf. Abstract, final sentence; column 2, lines 24-28). Therefore, it would

have been obvious to one of ordinary skills in the art to modify the invention of Hsia et al at the time it was made so as to include the further limitation of claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
November 17, 2003